



K26U 1174

Reg. No. : .....

Name : .....

IV Semester B.Sc. Degree (C.B.C.S.S. – O.B.E. – Supplementary/  
Improvement) Examination, April 2026  
(2023 Admission)

**CORE COURSE IN ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING**  
**4B05 AIML : Digital Fundamentals and Computer Organization**

Time : 3 Hours

Max. Marks : 40

**PART – A**  
**(Short Answer)**

Answer **all** questions. **Each** question carries 1 mark.

1. What is the associative property in Boolean algebra ?
2. Define minterms and maxterms in Boolean functions.
3. What is the difference between a latch and a flip-flop ?
4. Name two types of shift registers and their applications.
5. What is memory addressing in computer architecture ?
6. Define cache hit and cache miss in cache memory.

**(6×1=6)**

**PART – B**  
**(Short Essay)**

Answer **any six** questions. **Each** question carries 2 marks.

7. Explain De Morgan's theorems and their importance in Boolean algebra.
8. What are the differences between a half adder and a full adder ?
9. Describe the functionality of an SR flip-flop with a truth table.
10. Compare serial and parallel data transfer methods in digital systems.
11. Explain the concept of instruction encoding in computer architecture.

**P.T.O.**



12. What are structural hazards in pipelining and how do they affect performance ?
13. Describe the interrupt-driven I/O mechanism and its advantages.
14. Explain the LRU (Least Recently Used) algorithm for cache replacement. (6×2=12)

PART – C  
(Essay)

Answer **any four** questions. **Each** question carries **3** marks.

15. Discuss the importance of Karnaugh Maps (K-Map) in digital logic design and demonstrate simplification with an example.
16. Explain the working of synchronous and asynchronous counters with examples.
17. What are the different types of Instruction Set Architectures (ISA) ? Provide examples.
18. Discuss the role of pipelining in improving processor performance with an example.
19. What is Direct Memory Access (DMA) and how does it improve system performance ?
20. Explain the role of cache mapping techniques (Direct, Associative, Set-Associative) in cache memory. (4×3=12)

PART – D  
(Long Essay)

Answer **any two** questions. **Each** question carries **5** marks.

21. Explain the design and working of combinational logic circuits such as multiplexers, encoders and decoders.
  22. Describe the key components of computer architecture and their interconnections.
  23. Explain the concept of pipelining.
  24. Explain the various types of memory (SRAM, DRAM, ROM, Cache) and their impact on computer performance. (2×5=10)
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